OIPE IAP97
JUN 05 2006
PATENT & TRADEMARK OFFICE

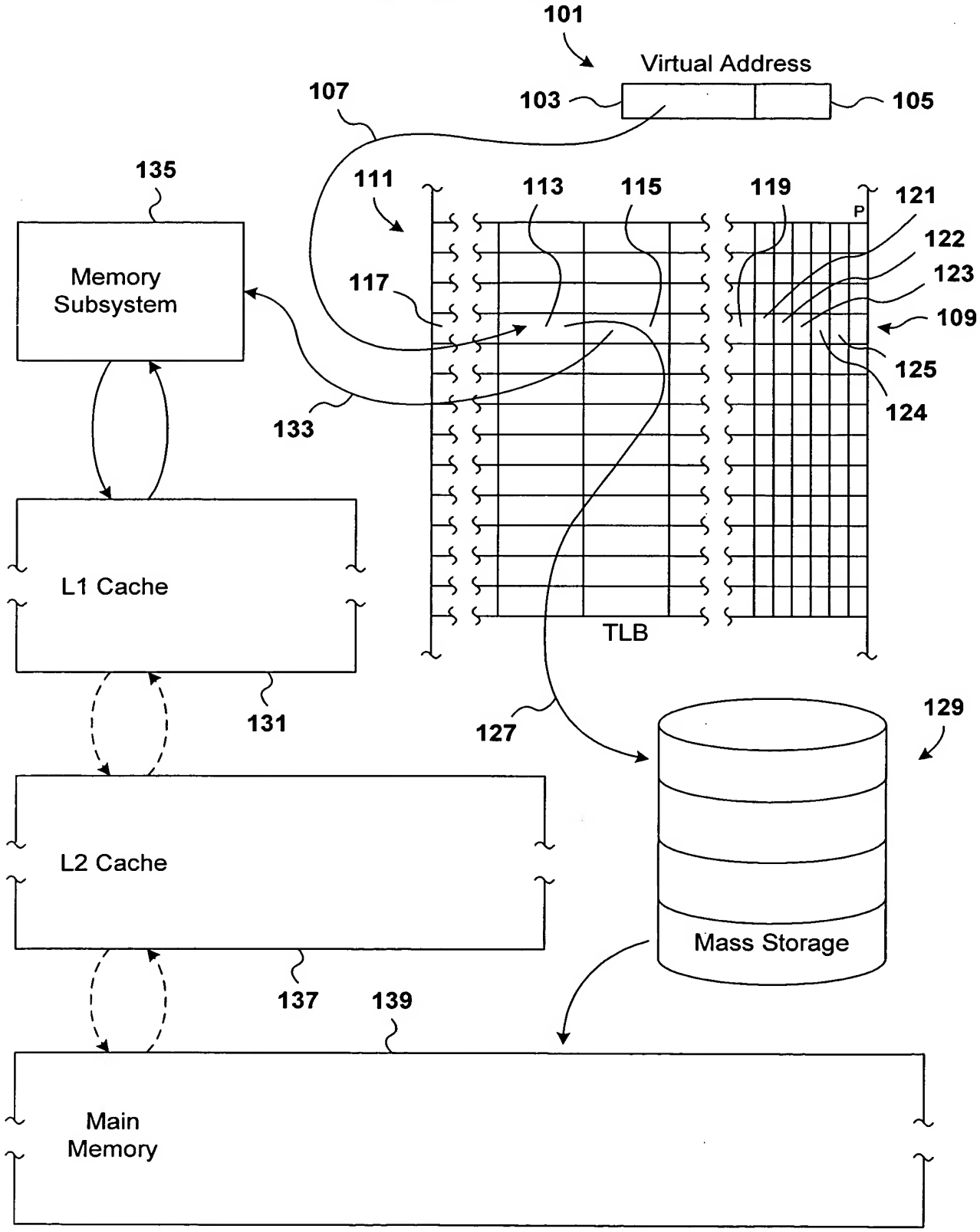

Figure 1
– Prior Art –

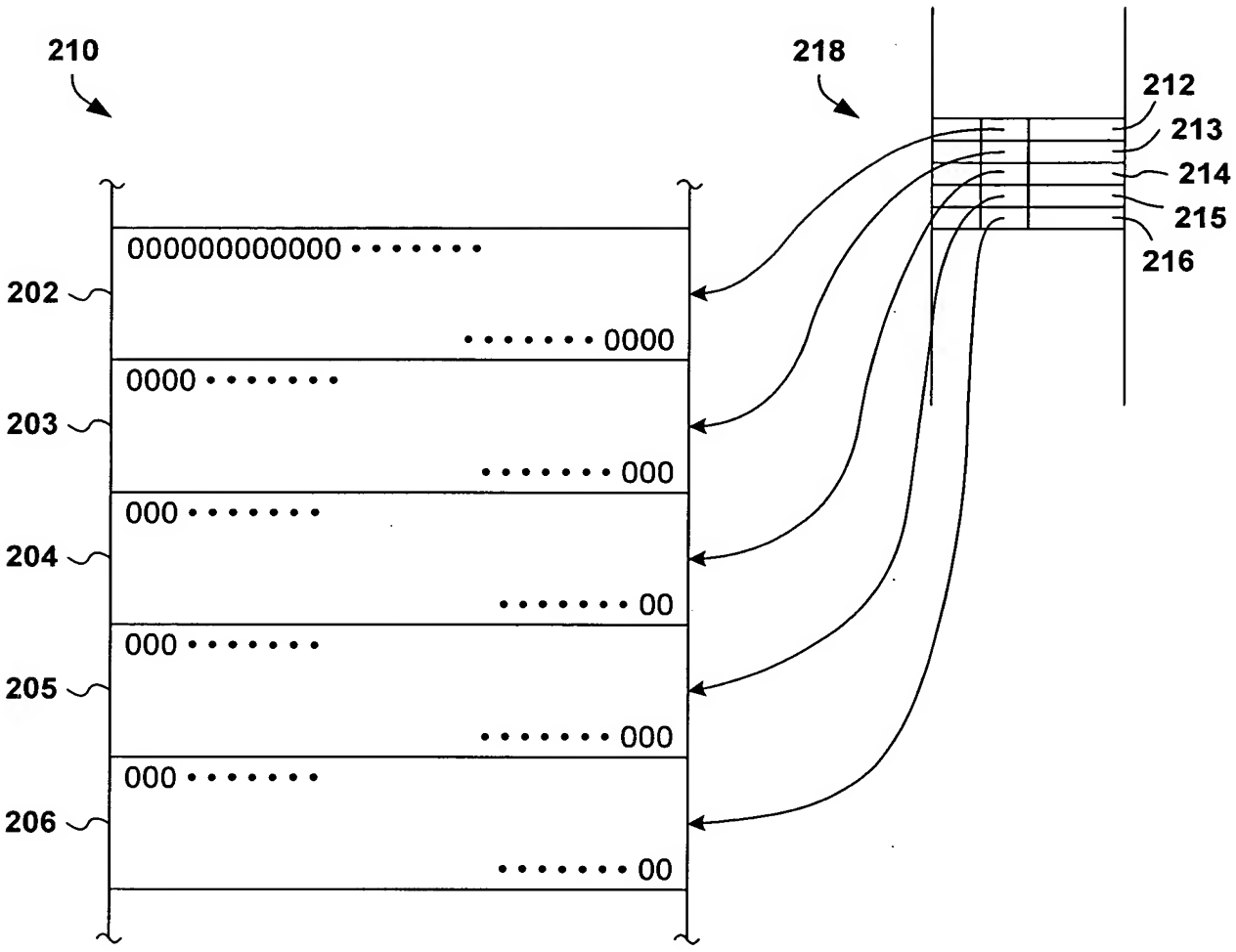

Figure 2
– Prior Art –

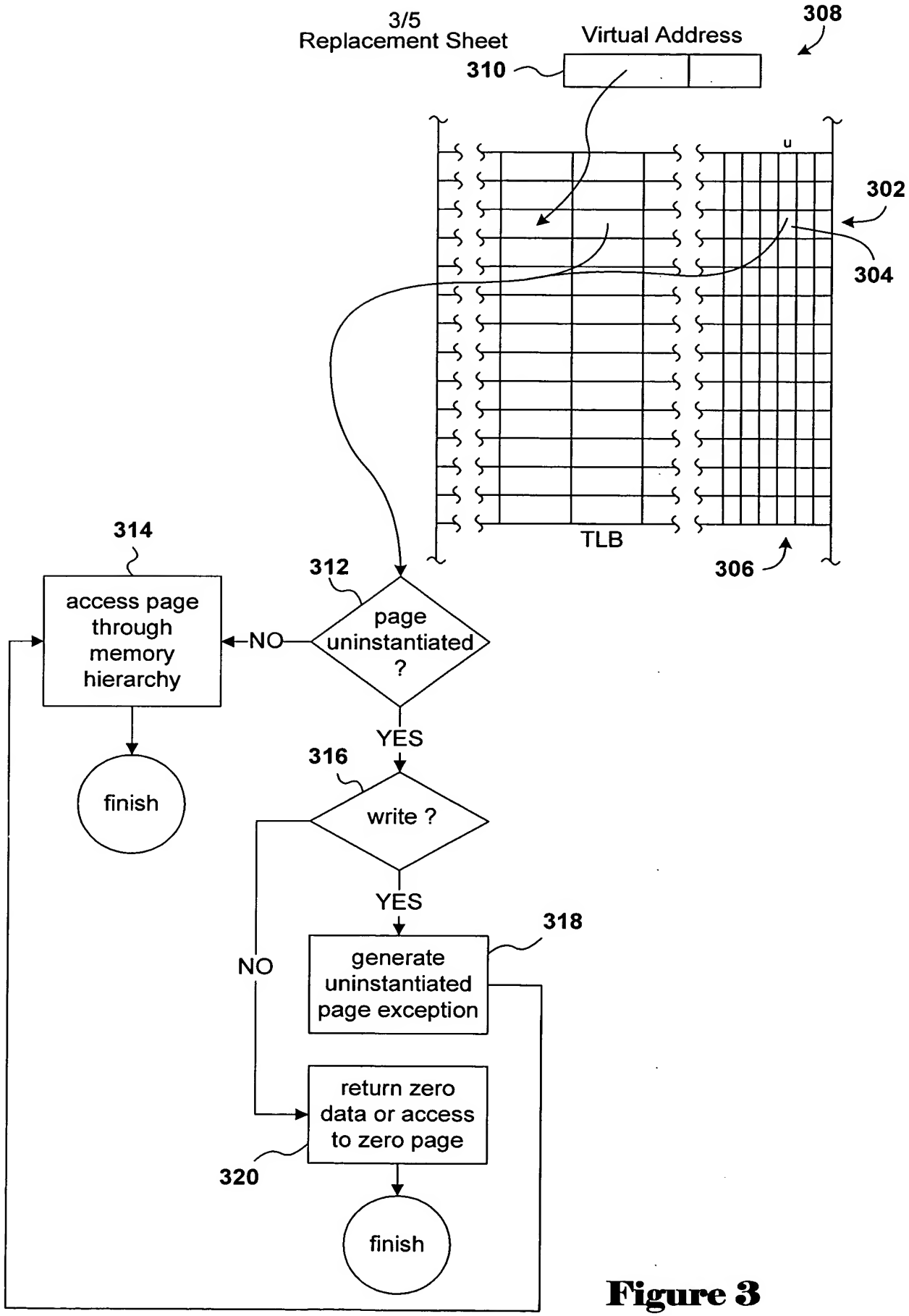
308
Virtual Address
310
u
302
304
TLB
306
314
312
access page through memory hierarchy
NO
page uninstantiated ?
YES
316
finish
write ?
YES
318
NO
generate uninstantiated page exception
return zero data or access to zero page
320
finish

Figure 3

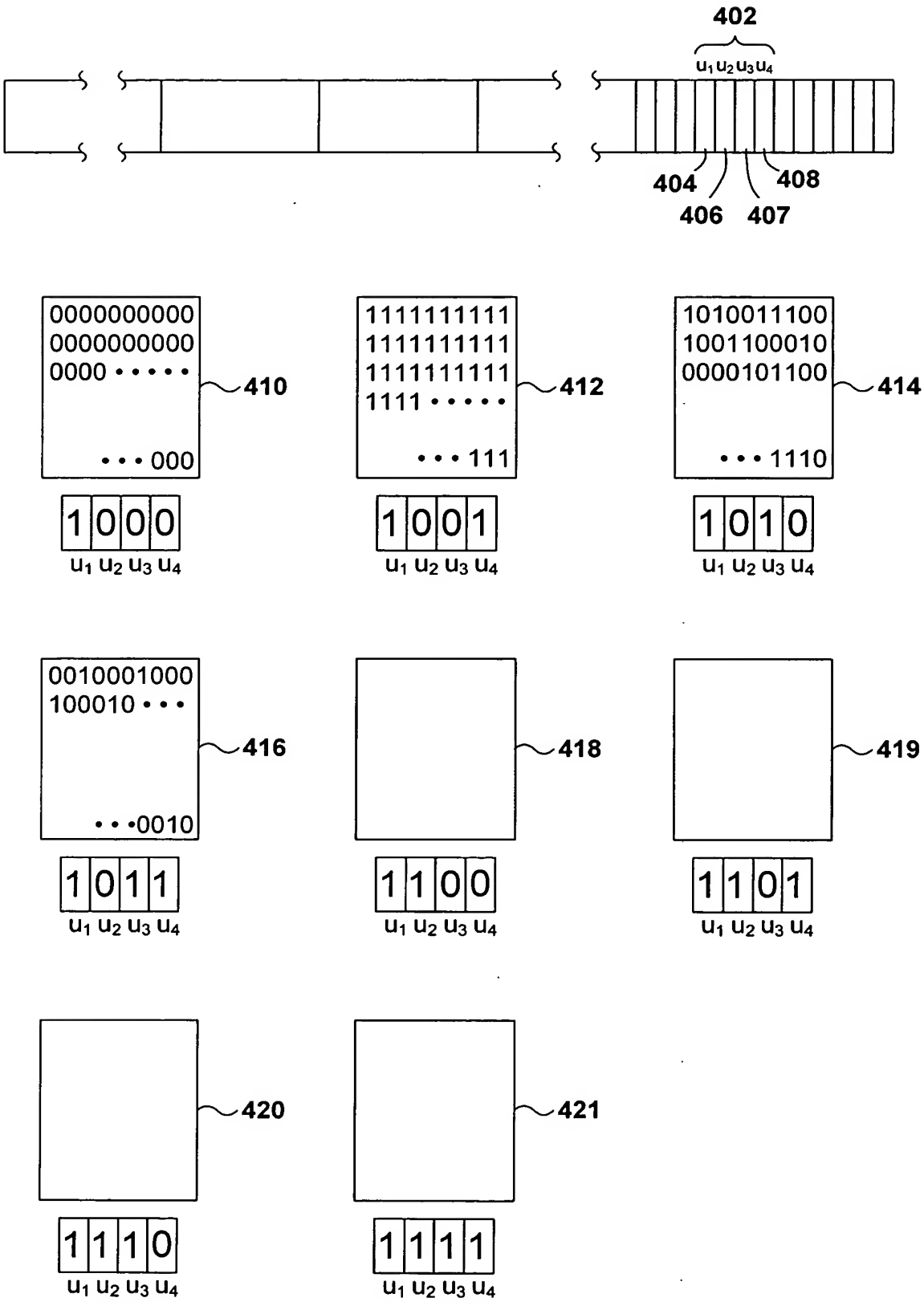
402
u1 u2 u3 u4
404
406
407
408
0000000000
0000000000
0000 • • • • •
• • • 000
410
1111111111
1111111111
1111111111
1111 • • • • •
• • • 111
412
1010011100
1001100010
0000101100
• • • 1110
414
1 0 0 0
u1 u2 u3 u4
1 0 0 1
u1 u2 u3 u4
1 0 1 0
u1 u2 u3 u4
0010001000
100010 • • •
• • •0010
416
418
419
1 0 1 1
u1 u2 u3 u4
1 1 0 0
u1 u2 u3 u4
1 1 0 1
u1 u2 u3 u4
420
421
1 1 1 0
u1 u2 u3 u4
1 1 1 1
u1 u2 u3 u4

Figure 4

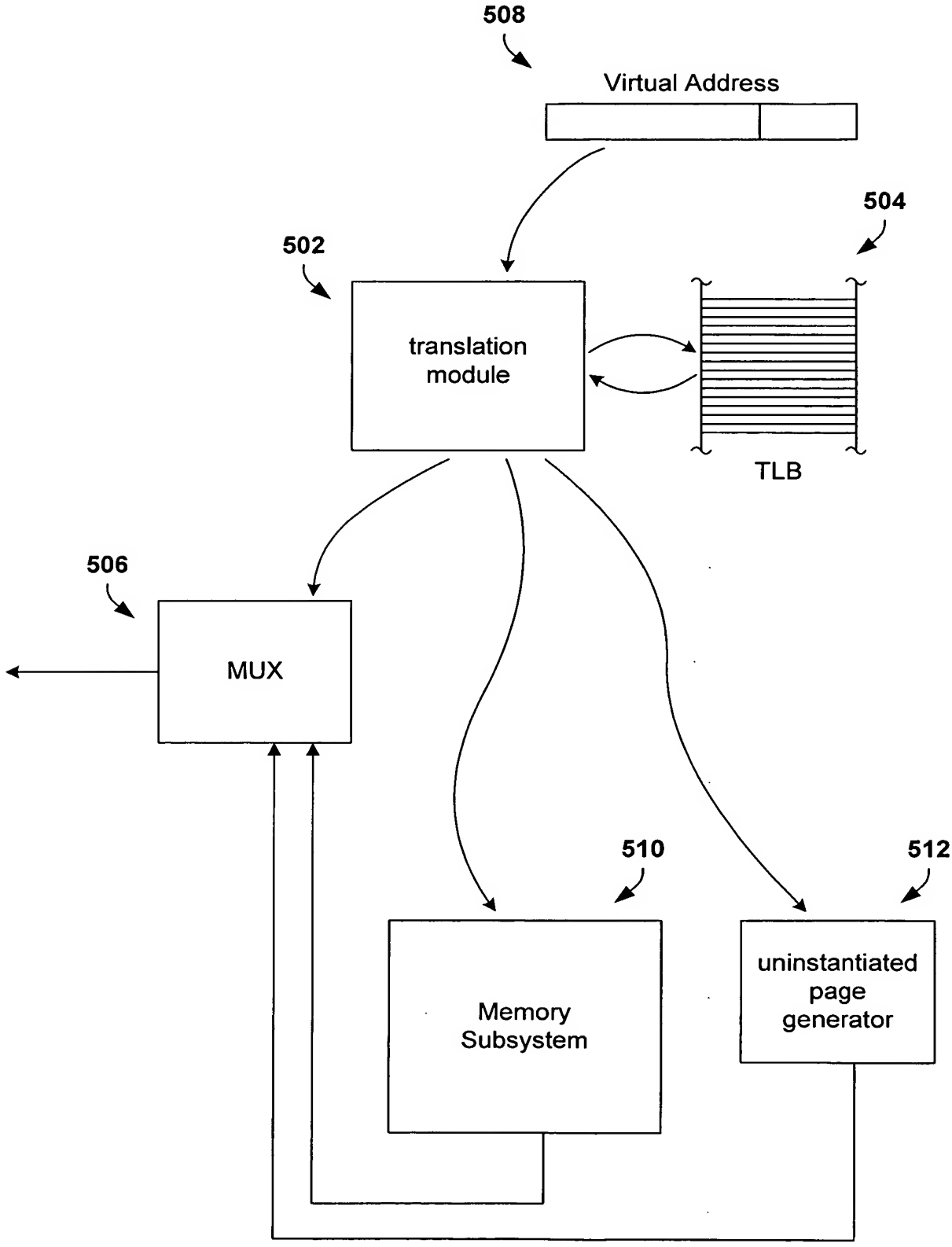
508
Virtual Address
504
502
translation module
TLB
506
MUX
510
512
Memory Subsystem
uninstantiated page generator

Figure 5